

REMARKS

Claims 1, 2, 6, 7, 9, 12-14, and 27 are pending in the application.

Claims 1, 2, 6, 7, 9, 12-14, and 27 are currently amended with claim 1 being an independent claim and claims 2, 6, 7, 9, 12-14, and 27 being dependent claims.

Applicants respectfully submit that no new matter is added to currently amended claims 1, 2, 6, 7, 9, 12-14, and 27. Claims 3-5, 8, 10, 11, 15-26, and 28-36 are cancelled.

Claims 1-2, 6-9, 12-14, and 26-36 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,506,642 to Luning et al., hereinafter, Luning, in view of U.S. Patent No. 6,258,680 to Fulford et al., hereinafter, Fulford.

Applicants respectfully traverse the rejection based on the following discussion.

I. The 35 U.S.C. 103(a) Rejection over Luning and Fulford

1. The Luning Disclosure

Referring to Fig. 4, Luning discloses that shallow source/drain extensions 45, 46 are then formed in a conventional manner employing the gate electrodes 41 and 42 as masks. Subsequently, first sidewall spacer 44 is deposited on the side surfaces of the first and second gate electrodes 41, 42. Sidewall spacer 44 has a width W_1 typically of about 600 to 1,200 Å. (col. 4, lines 45-50).

Luning also discloses that subsequently, as schematically illustrated in Fig. 5, a photoresist mask 50 is formed over the second gate electrode 42, inclusive of the first sidewall spacers 44 and etching is conducted to remove the first sidewall spacers 44 from the side surfaces of the first gate electrode. (col. 4, lines 51-55).

Luning further discloses, it can be appreciated from Fig. 6 that the width of the second sidewall spacer W_2 selectively controls the length of the source/drain extension of the n-MOS transistor, while the thickness of the first and second sidewall spacers W_3 , typically about 900 Å to 1,500 Å, controls the length of the source/drain extension of the p-MOS transistor. (col. 4, line 64 to col.5, line 3).

2. The Fulford Disclosure

Fulford discloses that an oxide layer 128 is to act as an etch stop during subsequent formation and removal of a spacer material set forth below. The spacer is preferably nitride and, since nitride and oxide have different etch characteristics, the spacer can be formed and removed separate from the underlying oxide. (col. 8, lines 17-22)

3. Arguments

Currently amended, independent claim 1 recites in relevant part,
"first impurity source/drain implant regions formed, in said substrate,
substantially adjacent to outer edges of said first spacer formed on said sidewalls of said NFET gate conductor;

...

second impurity source/drain implant regions formed, in said substrate,
substantially adjacent to outer edges of said second spacer formed on said sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor".

Referring to Fig. 6, Luning merely discloses shallow source/drain extensions 45, 46 that are formed in a conventional manner employing the gate electrodes 41 and 42 as masks. Therefore, as shown in Fig. 6, the shallow source/drain extension 46 of the n-MOS transistor extends from the sidewall of the gate electrode 41, underneath the second sidewall spacer 60 and beyond, whereas the shallow source/drain extension 45 of the p-MOS transistor extends from the sidewall of the gate electrode 42, underneath the first and second spacers 44, 66 and beyond. The source/drain extension regions of Luning extend from the sidewalls of the gate electrodes, because the gate electrodes are used as the mask during ion implantation.

In contrast, the present invention describes at least the features of: the first impurity source/drain implant region of the NFET extends from an outer edge of a first spacer formed on sidewalls of the NFET gate conductor and the second impurity

source/drain region extends from an outer edge of a second spacer formed on said sidewalls of the first spacer, which is formed on the sidewalls of the PFET gate conductor. In the present invention, ion implantation occurs after formation of the first spacer for the NFET; hence, the first spacer is part of the mask for ion implantation of the NFET. While ion implantation occurs after formation of the first and second spacers for the PFET; hence, the first and second spacers are part of the mask for ion implantation of the PFET.

For at least the reasons outlined above, Applicants respectfully submit that Luning does not disclose, teach or suggest at least the present invention's features of "first impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said first spacer formed on said sidewalls of said NFET gate conductor; ... second impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said second spacer formed on said sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor", as recited in currently amended, independent claim 1.

Fulford does not cure the deficiencies of Luning.

Fulford merely discloses that an oxide layer may act as an etch stop during subsequent formation and removal of a spacers.

Nowhere does Fulford disclose, teach or suggest at least the present invention's features of "first impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said first spacer formed on said sidewalls of said NFET gate conductor; ... second impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said second spacer formed on said sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor", as recited in currently amended, independent claim 1.

Instead, Fulford merely discloses that an oxide layer may act as an etch stop during subsequent formation and removal of a spacers.

For at least the reasons outline above with respect to the rejection of the claims over Luning and for at least the reasons outlined immediately able with respect to the rejection of the claims over Fulford, Applicants respectfully submit the Luning and Fulford, either individually or in combination, do not disclose, teach or suggest at least the present invention's features of "first impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said first spacer formed on said sidewalls of said NFET gate conductor; ... second impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said second spacer formed on said sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor", as recited in currently amended, independent claim 1. Accordingly, Luning and Fulford, either individually or in combination, fail to render obvious the subject matter of currently amended, independent claim 1 and currently amended, dependent claims 2, 6, 7, 9, 12-14, and 27 under 35 U.S.C. §103(a). The rejection of cancelled claims 8 and 28-36 is moot. Withdrawal of the rejection of claims 1-2, 6-9, 12-14, and 26-36 under 35 U.S.C. §103(a) as unpatentable over Luning in view of Fulford is respectfully solicited.

II. Formal Matters and Conclusion

Claims 1, 2, 6, 7, 9, 12-14, and 27 are pending in the application.

With respect to the rejection of the claims over the prior art, Applicants respectfully submit that currently amended claims 1, 2, 6, 7, 9, 12-14, and 27 are distinguishable over the prior art of record. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejection to the claims.

In view of the foregoing, Applicants submit that claims 1-2, 6-9, 12-14, and 26-36, all the claims presently pending in the application, are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest time possible.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

Dated: April 28, 2008

/Peter A. Balnave/

Peter A. Balnave, Ph.D.

Registration No. 46,199

Gibb & Rahman, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-5255
Fax: (301) 261-8825
Email: Balnave@Gibb-Rahman.com
Customer Number: 29154